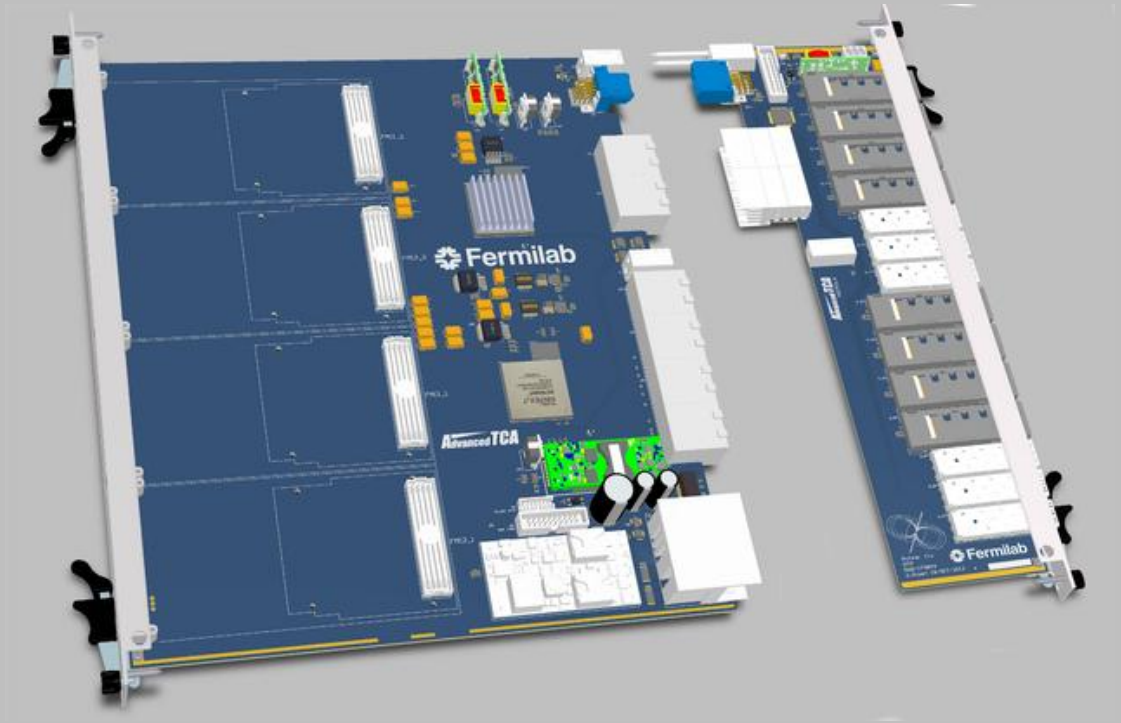


Pulsar-IIa Design Review

14 November 2012

Jamieson Olsen, Yasu Okumura, Ted Liu

Outline

- Brief introduction to ATCA
- Pulsar IIa Prototype Board
  - Block diagram
  - ATCA management microcontroller
  - FPGA programming and slow controls
  - Power distribution
  - Controlled impedance and PCB stackup
- On to the schematics and PCB…

Prototype Goals

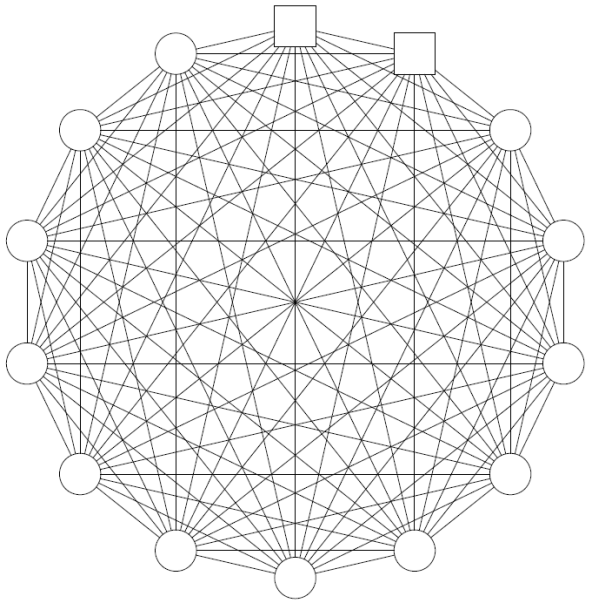
- Confirm ATCA board compliance
  - Board mechanics
  - Power
  - IPMI management / microcontroller
  - RTM Interface
- Test the Mezzanine Card Interface
- Test our firmware designs on Kintex FPGAs
  - GTX transceivers and LVDS serial I/O
  - DDR3 memory interface
- Verify that our PCB layout is clean
- Our Prototype board is very close to the target design but uses smaller FPGAs and fewer GTX transceivers

Advanced TCA

- Standards developed by Telecom for high availability
- 14 slot backplane
- 48VDC Power, hot swap
- Rear Transition Modules
- Platform management bus based on I2C
- Redundant shelf manager boards

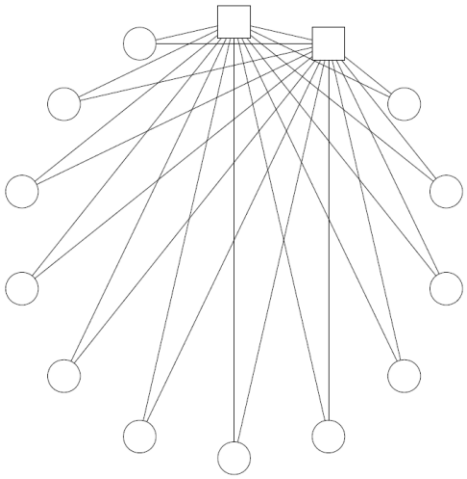
Fabric Interface

- Full mesh
- 1 channel = 4 full duplex ports
- Up to 10Gbps per port
- 100 ohm differential pairs
- Protocol Agnostic
- 8B/10B serial transmission

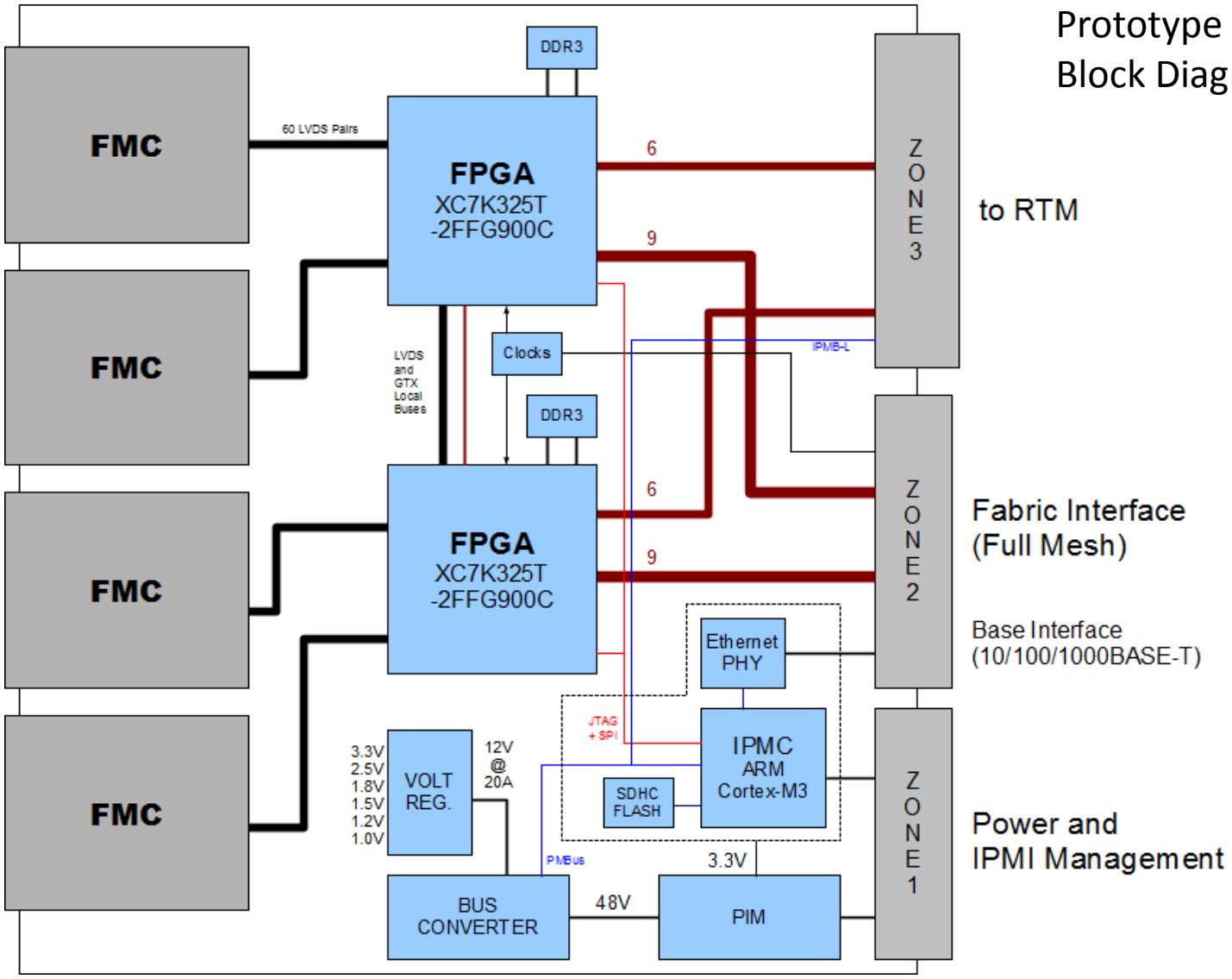


Base Interface

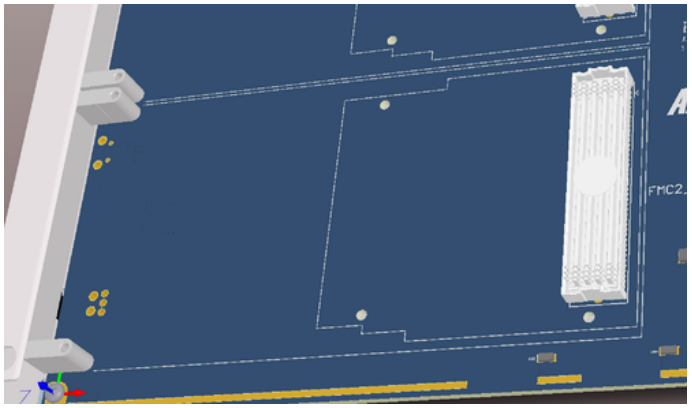
- Dual Star
- Slots 1 and 2 are hubs
- 10/100/1000BASE-T Ethernet
- We plan to use 100BASE-T for slow controls, board status, firmware downloading, etc.
- Commercial blades include Ethernet switch + optional CPU

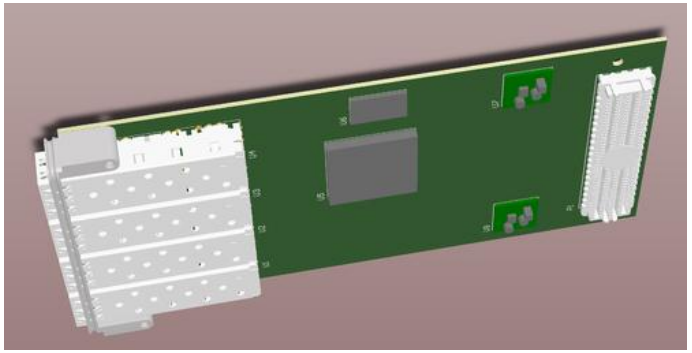


Prototype Board Block Diagram



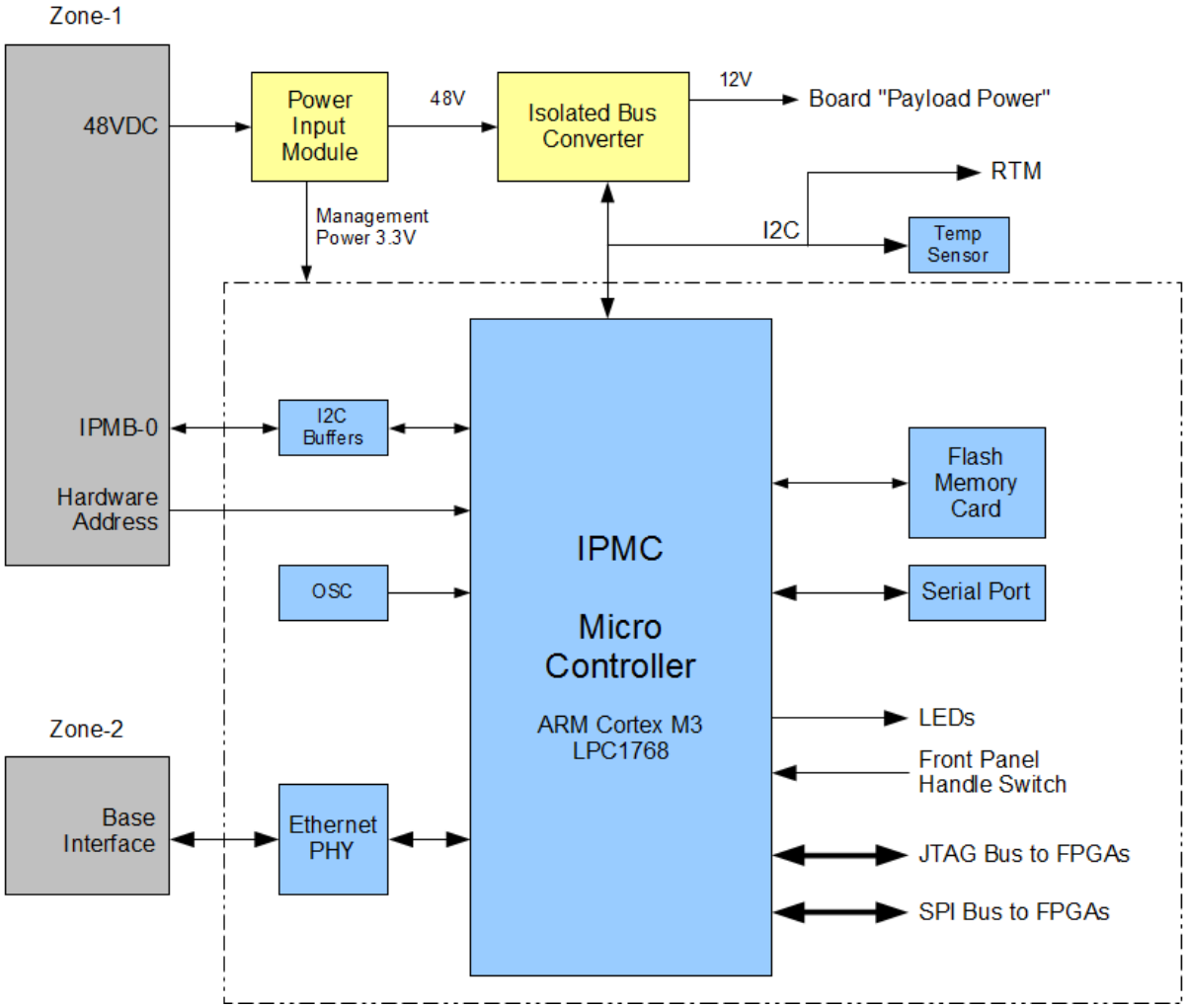
Mezzanine Cards



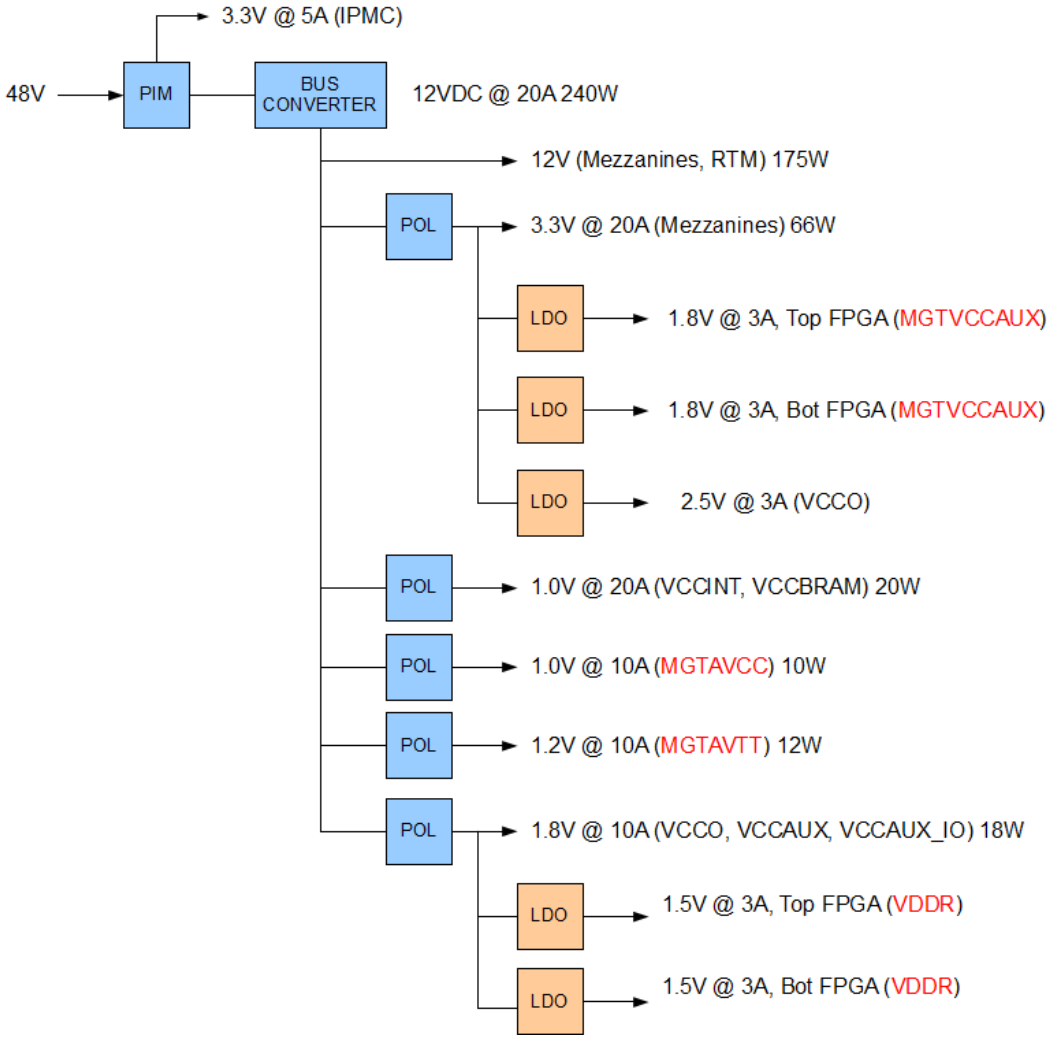


- VITA57 **FMC** Specification
- 74 x 149mm (PMC size)
- High (400) and Low (160) pin count connector:
  - 2 output clocks (LVDS)
  - 58 user defined signals (LVDS)
  - I2C management and JTAG
  - +12V and +3.3V Power
  - No GTX/MGT serial I/O
- 72Gbps max bandwidth
- Xilinx / Digilent dev boards

Microcontroller Detail



Power Distribution

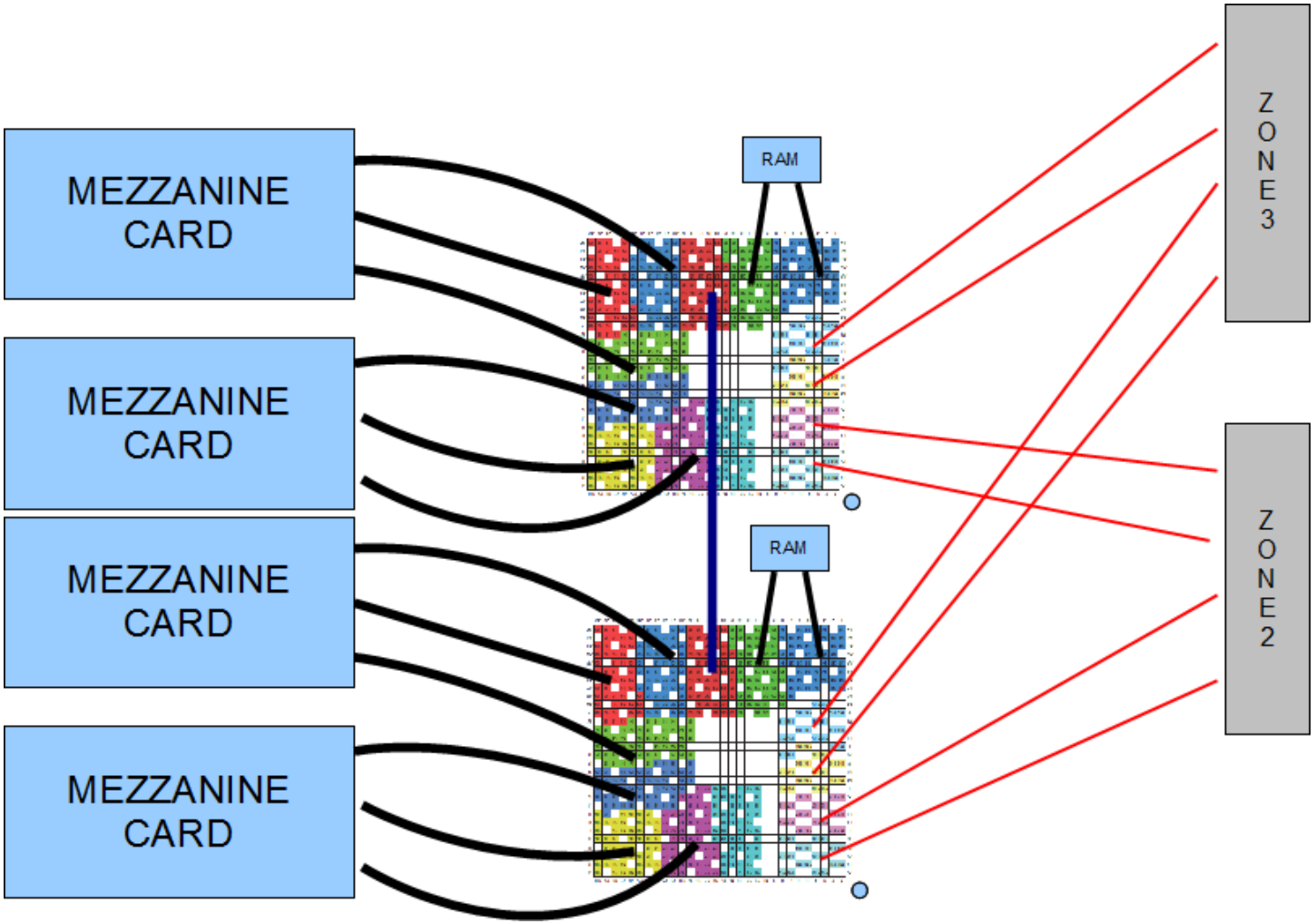


FPGA power estimate = 11W
(Worst Case)

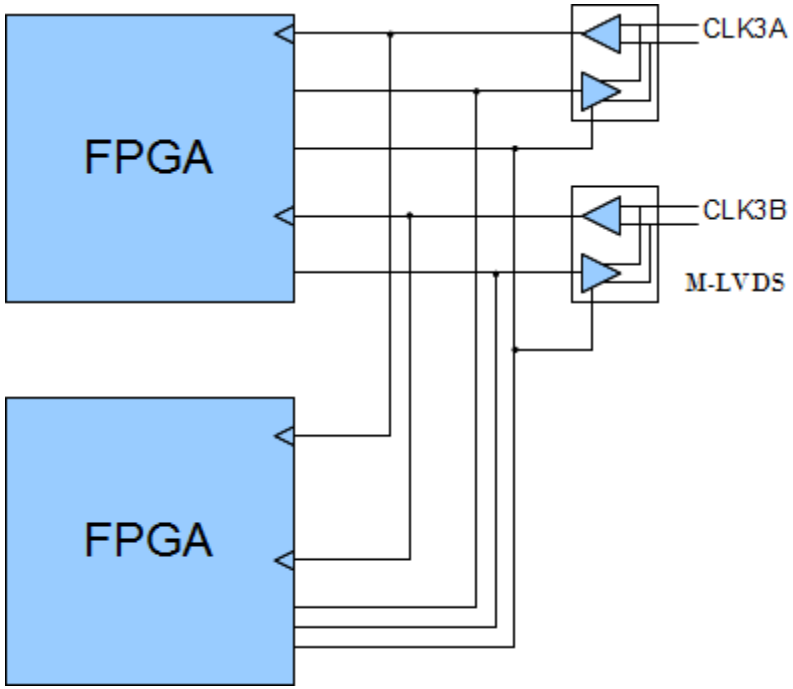
Power Supply

Source	Voltage	Total (A)
V_{CCINT}	1.000	2.475
V_{CCBRAM}	1.000	0.046
V_{CCAUX}	1.800	0.778
V_{CCAUX_IO}	2.000	
V_{CCO} 3.3V	3.300	0.003
V_{CCO} 2.5V	2.500	1.269
V_{CCO} 1.8V	1.800	0.076
V_{CCO} 1.5V	1.500	0.155
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
$MGTV_{CCAUX}$	1.800	0.041
$MGTAV_{CC}$	1.000	2.736
$MGTAV_{TT}$	1.200	1.347
-		
-		
-		

FPGA Banks

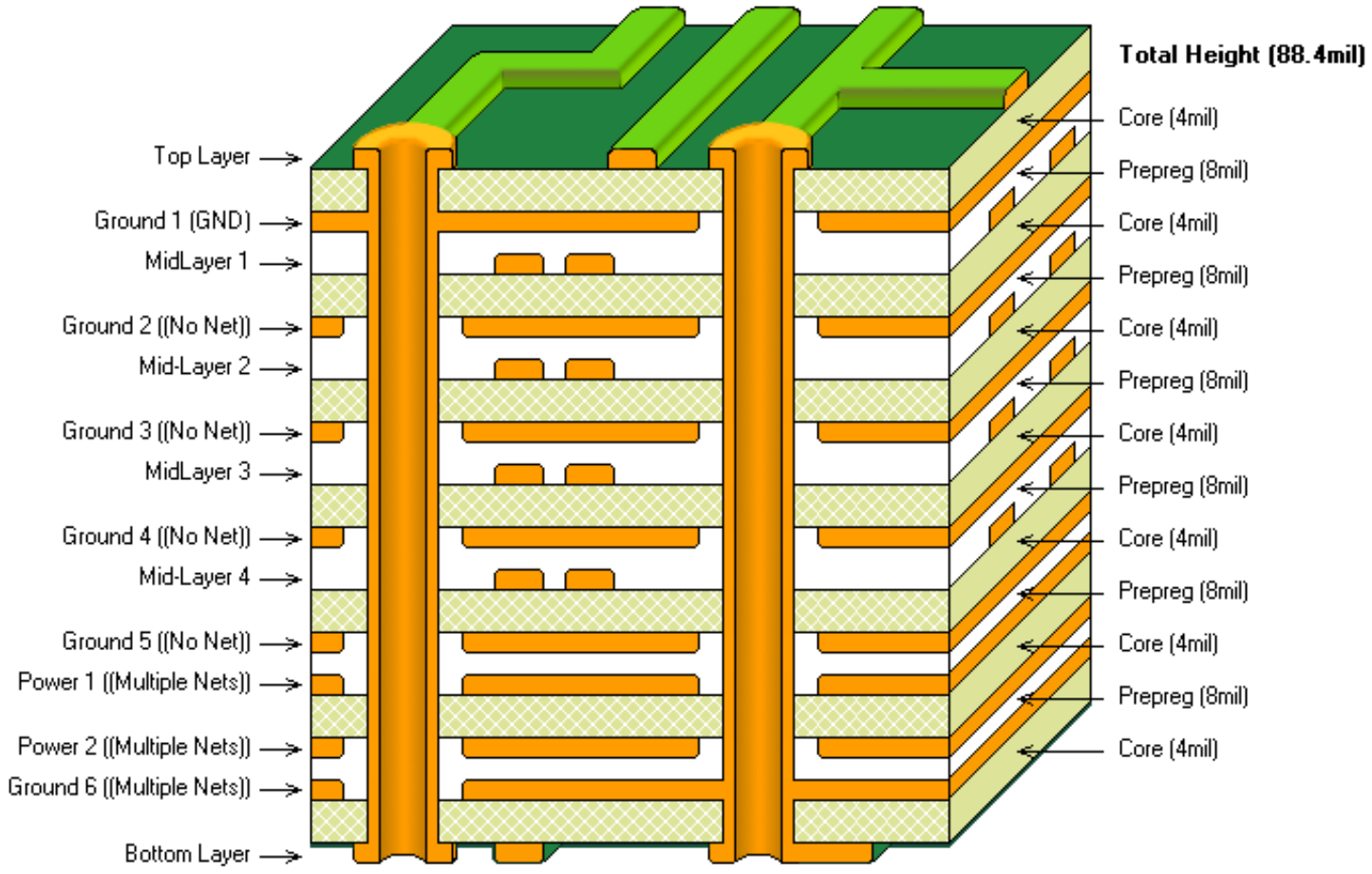

MEZZANINE CARD
MEZZANINE CARD
MEZZANINE CARD
MEZZANINE CARD
RAM
RAM
ZONE 3
ZONE 2

Backplane Clocks



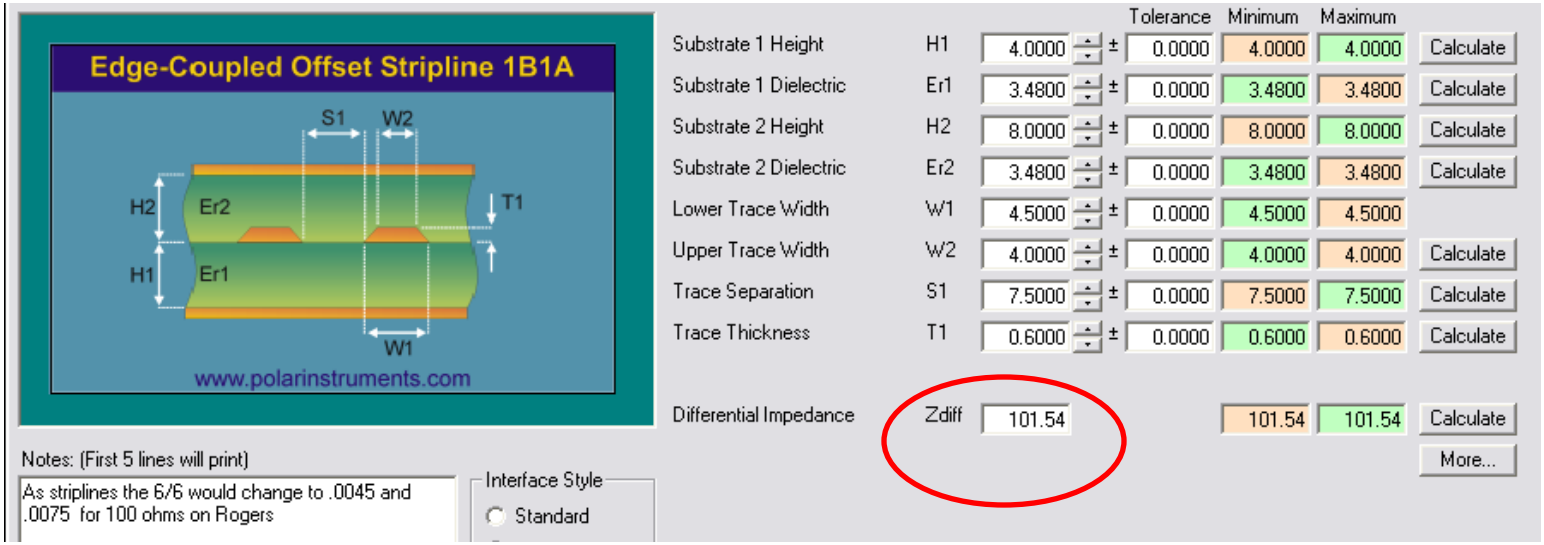
- 6 clocks are bussed used to all slots
- CLK3A and CLK3B are user-defined
- Each FPGA has the ability to drive CLK3A and CLK3B
- M-LVDS drivers
- Frequency < 100MHz
- Good for beam crossing, L1 accept, resets, etc.

14 Layer PCB

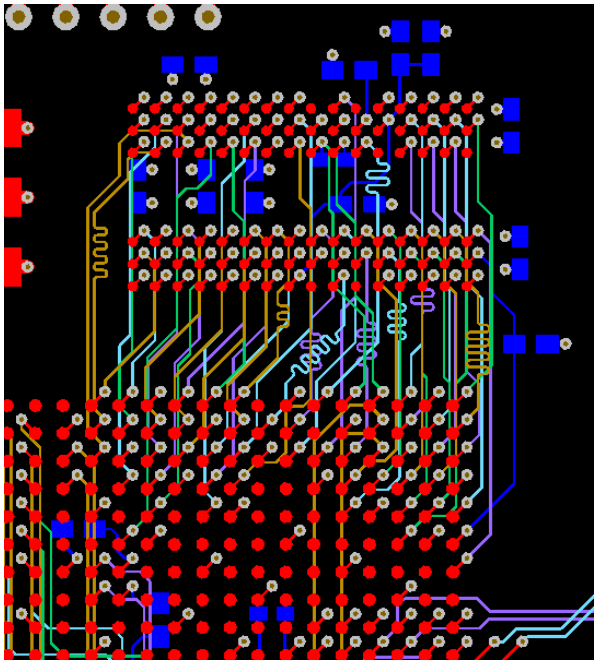

Total Height (88.4mil)
Top Layer
Ground 1 (GND)
MidLayer 1
Ground 2 ((No Net))
Mid-Layer 2
Ground 3 ((No Net))
MidLayer 3
Ground 4 ((No Net))
Mid-Layer 4
Ground 5 ((No Net))
Power 1 ((Multiple Nets))
Power 2 ((Multiple Nets))
Ground 6 ((Multiple Nets))
Bottom Layer
Core (4mil)
Prepreg (8mil)
Core (4mil)
Prepreg (8mil)
Core (4mil)
Prepreg (8mil)
Core (4mil)
Prepreg (8mil)
Core (4mil)
Prepreg (8mil)
Core (4mil)

Controlled Impedance

- GTX up to 10Gbps, LVDS up to 1.25Gbps
- 100 ohms differential on inner layers
- Top and Bottom are 50 ohms (but not as critical)
- Differential pairs are edge coupled striplines
- FR4 -> Rogers RO4350 material
- Using Prototron's recommendation:

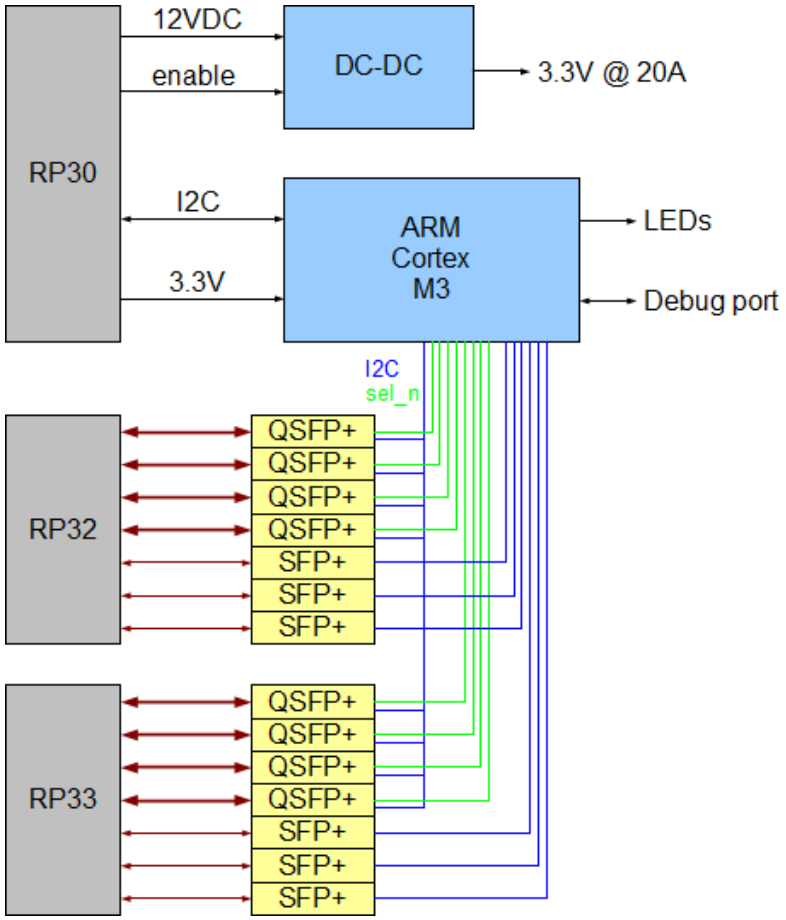


DDR3 Memory



- Single chip DDR3 256MB 16-bit
- Longest trace is ~20mm
- No termination resistors on Addr/control group
- 50 ohm traces
- Component is rated for 533MHz but we plan to run at 400MHz
  - 1.6GB/sec max
  - 1GB/sec sequential access (WP383)
- Signal length matching meets Xilinx guidelines (UG586)
- Pinout verified in latest Coregen

RTM Block Diagram



- ARM Cortex M3 is an MMC on the IPMB-L bus
- All SFP and QSFP modules have an I2C interface for control and status
  - Optical signal level, temperature, voltages, serial numbers, etc.